

## Electrical Engineer - ASIC Layout

This position will play a key role in the ASIC group of the Implant R&D department as the main layout engineer. He/she will work with ASIC circuit design engineers on architectural design and floor planning, and carry out most of the chip circuit layout work to ensure timely submission for fabrication of chip designs in various development phases of ASIC for visual prosthesis. Additionally, this position is responsible for PCB layout for chip testing circuits, and plays a supporting role in chip testing.

The main responsibilities include:

- Carry out block level circuit layout and chip level layout integration to ensure timely submission of ASIC's
- Work with design engineers on chip architectural designs, floor planning and pad frame decisions
- Carry out PCB layout for chip test circuits and implant test circuits
- Participate in chip evaluation and verification testing and other implant related testing
- Maintain CAD software for chip layout

Qualifications:

- EE BSc degree with at least four years of experience or MSc degree with at least two years of experience in comprehensive CMOS chip layout work that includes chip level layout, DRC and LVS
- Good understanding of CMOS fabrication processes
- Good understanding of principles of CMOS devices and circuits
- Experience in high voltage CMOS circuit layout a plus
- Experience with Tanner software a plus
- PCB layout experience a plus
- Experience with maintaining CAD software a plus